

REMARKS

Claims 61, 63 and 65 have been canceled. Claims 59 and 92 have been amended. No new matter has been introduced. Claims 94 and 95 have been added to round out the scope of protection afforded by the present invention. Claims 59-60, 62, 64, 66-84 and 92-95 are now pending.

Response to rejection under 35 U.S.C. § 102(b)

Claims 59-65, 67-84, 92 and 93 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Summerfelt et al. (U.S. Patent No. 5,612,574) ("Summerfelt"). This rejection is respectfully traversed.

The claimed invention relates to a integrated circuit structure with specific structural features obtained by a particular process methodology. As such, amended independent claim 59 recites an "integrated circuit substrate" comprising *inter alia* "a substrate", "an oxide layer formed over said substrate" and "a plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes." As recited in claim 59, "said reduced sidewall striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma."

Amended independent claim 92 similarly recites an "integrated circuit substrate" comprising *inter alia* "a substrate", "an oxide layer formed over said substrate" and "a plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations." Claim 92 recites that the plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations result "from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined

time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma.” Claim 92 further recites that the “substrate has a decreased critical dimension loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma.”

Summerfelt relates to a semiconductor structure “using high-dielectric-constant materials and an adhesion layer.” (Abstract; Title). Summerfelt teaches that “an interlevel isolation layer” and a “barrier layer” are formed over the active region and “disposed outwardly from the conductive plug.” (Col. 2, lines 42-46). “[A]n oxygen-stable inner electrode is formed outwardly from portions of the interlevel isolation layer and the barrier layer.” (Col. 2, lines 46-48). Summerfelt also teaches that “[A]n adhesion layer is disposed between the oxygen-stable inner electrode and the interlevel isolation layer and the barrier layer.” (Col. 2, lines 48-51). In this manner, “the problems of adhesion between the oxygen-stable layer and the interlayer isolation layer in devices including such materials” are eliminated. (Col. 2, lines 29-32).

Summerfelt does not disclose the limitations of claims 59-60, 62, 64, 66-84 and 92-95. Summerfelt is silent about a “integrated circuit substrate” comprising “an oxide layer formed over said substrate” and “a plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes.” Summerfelt does not teach or suggest the claimed feature of a substrate having a reduced or decreased critical dimension loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma.

For at least these reasons, Summerfelt fails to disclose all limitations of claims 59-60, 62, 64, 66-84 and 92-95 and withdrawal of this rejection is respectfully requested.

Claims 59-61, 64-66, 68-84, 92 and 93 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Filipiak et al. (U.S. Patent No. 6,054,377) (“Filipiak”). This rejection is respectfully traversed.

Filipiak relates to a method for forming an inlaid via in a semiconductor device, and methods for making a semiconductor device (Abstract; Title). Filipiak teaches a semiconductor device 30 which includes “a semiconductor substrate 32 having an overlying dielectric layer 34 and a metal interconnect 36.” (Col. 3, lines 43-46). “[A] first interlayer dielectric (ILD) 40 overlies interconnect 36. ...The thickness of ILD 40 should be chosen such that a via can be etched through the dielectric material over interconnect 36 and that a conductive material can be successfully deposited in such via opening.” (Col. 4, lines 29-30 and 37-40). Filipiak also teaches that “after depositing etchstop layer 42, device 30 is patterned and etched to form a contact or via opening 44 through etchstop layer 42 and into ILD 40” and “via opening 44 exposes a portion of interconnect 36, namely that portion of the interconnect which is to be contacted by a subsequently deposited metal layer.” (Col. 4, lines 51-56). Filipiak teaches that after formation of interlayer dielectric (ILD) 45, and “following formation of trench opening 48, a metal layer 50 is deposited over device 30” (Col.5, lines 65-66) such that “the resulting interconnect structure will have a trench portion 52 and a via portion 54” (Col.6, lines 10-15).

Like Summerfelt, Filipiak is silent about a “integrated circuit substrate” comprising “an oxide layer formed over said substrate” and “a plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes.,“ as recited in independent claim 59. With respect to independent claim 92, Filipiak does not teach or suggest the claimed feature of a substrate having a reduced or decreased critical dimension loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma.

For at least these reasons, Filipiak fails to disclose all limitations of claims 59-60, 62, 64, 66-84 and 92-95, and withdrawal of this rejection is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By

Stephen A. Soffen

Registration No.: 31,063

Gabriela I. Coman

Registration No.: 50,515

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorneys for Applicant

Version With Markings to Show Changes Made

59. (Twice Amended) A integrated circuit substrate [formed by a method], comprising:

a substrate;

an oxide layer formed over said substrate; and

a plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes, said reduced sidewall striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time

[placing said integrated circuit substrate into a reactive chamber;

introducing into said chamber an etching gas;

generating a plasma of said etching gas at a first power level and

contacting said substrate with said first power level plasma for a first predetermined time; and

generating a plasma of said etching gas at a second power level in said chamber and contacting said integrated circuit substrate with said second power level plasma for a second predetermined time], wherein said second power level plasma is a higher power plasma than said first power level plasma.

92. (Amended) A integrated circuit substrate [formed by a method], comprising [the steps of]:

a substrate;

an oxide layer formed over said substrate; and

a plurality of cylindrical contact holes formed in said oxide layer having reduced sidewall striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the

application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time

[(a) placing said integrated circuit substrate into a reactive chamber;
(b) introducing an etching gas into said chamber;
(c) generating a plasma of said etching gas at a first power level and contacting said substrate with said first power level plasma for a first predetermined time; and
(d) generating a plasma of said etching gas at a second power level in said chamber and contacting said integrated circuit substrate with said second power level plasma for a second predetermined time], wherein said second power level plasma is a higher power plasma than said first power level plasma, and wherein said substrate has a decreased critical dimension [CD] loss [decreased] compared to the critical dimension [CD] loss of a substrate formed [by a method comprising said steps (a), (b) and (c) but not step (d)] without the application of the second, higher power level plasma.